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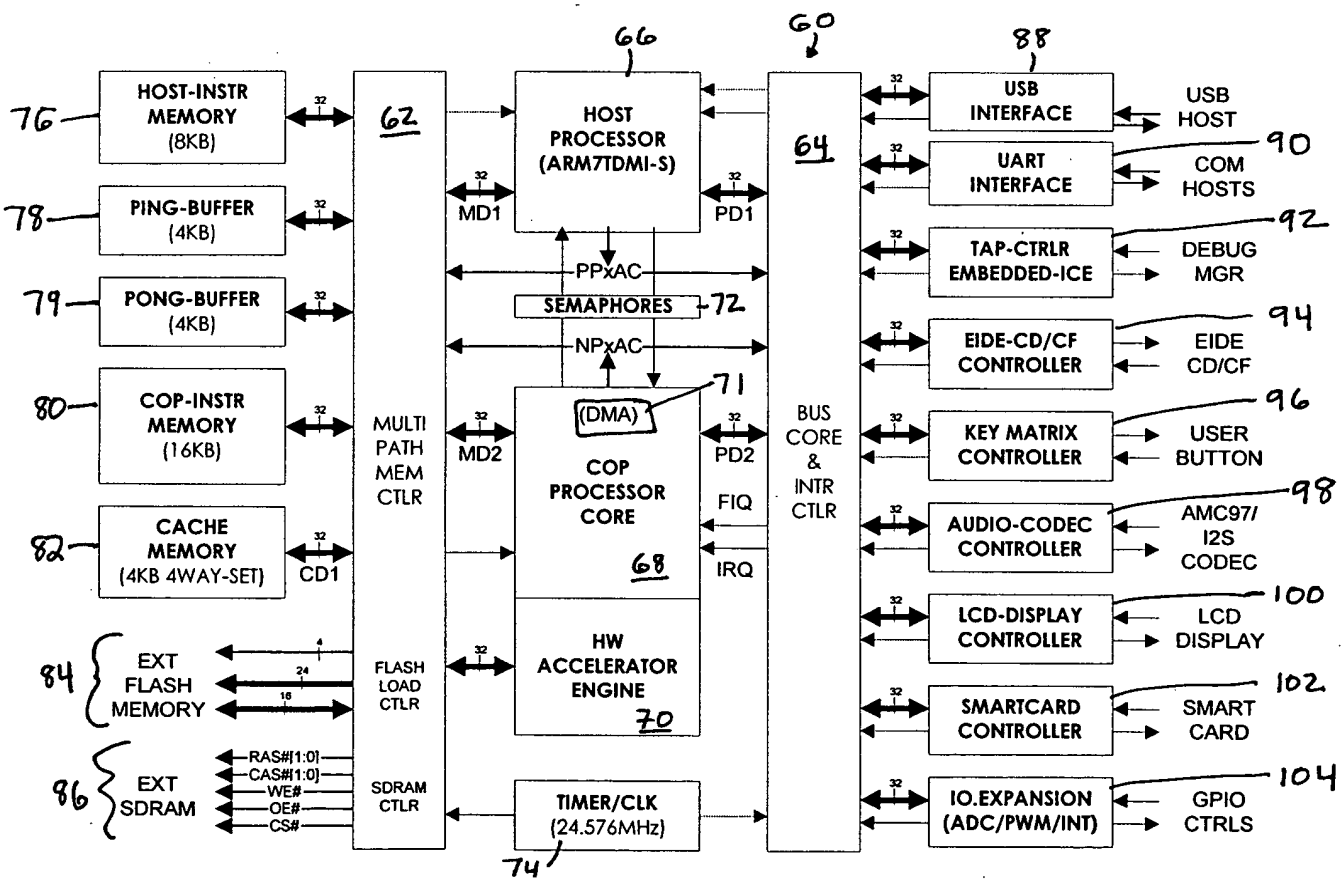
HOST-INSTR MEMORY (8KB)
PING-BUFFER (4KB)
PONG-BUFFER (4KB)
COP-INSTR MEMORY (16KB)
CACHE MEMORY (4KB 4WAY-SET)
EXT FLASH MEMORY
EXT SDRAM
RAS#[1:0]
CAS#[1:0]
WE#
OE#
CS#
MULTI PATH MEM CTLR
FLASH LOAD CTLR
SDRAM CTLR
CD1
MD1
MD2
PD1
PD2
HOST PROCESSOR (ARM7TDMI-S)
PPxAC
SEMAPHORES
NPxAC
(DMA)
COP PROCESSOR CORE
HW ACCELERATOR ENGINE
TIMER/CLK (24.576MHz)
FIQ
IRQ
BUS CORE & INTR CTLR
USB INTERFACE
UART INTERFACE
TAP-CTRLR EMBEDDED-ICE
EIDE-CD/CF CONTROLLER
KEY MATRIX CONTROLLER
AUDIO-CODEC CONTROLLER
LCD-DISPLAY CONTROLLER
SMARTCARD CONTROLLER
IO.EXPANSION (ADC/PWM/INT)
USB HOST
COM HOSTS
DEBUG MGR
EIDE CD/CF
USER BUTTON
AMC97/ I2S CODEC
LCD DISPLAY
SMART CARD
GPIO CTRLS
76
78
79
80
82
84
86
62
66
60
64
88
90
92
94
96
98
100
102
104
72
71
68
70
74

FIGURE 1

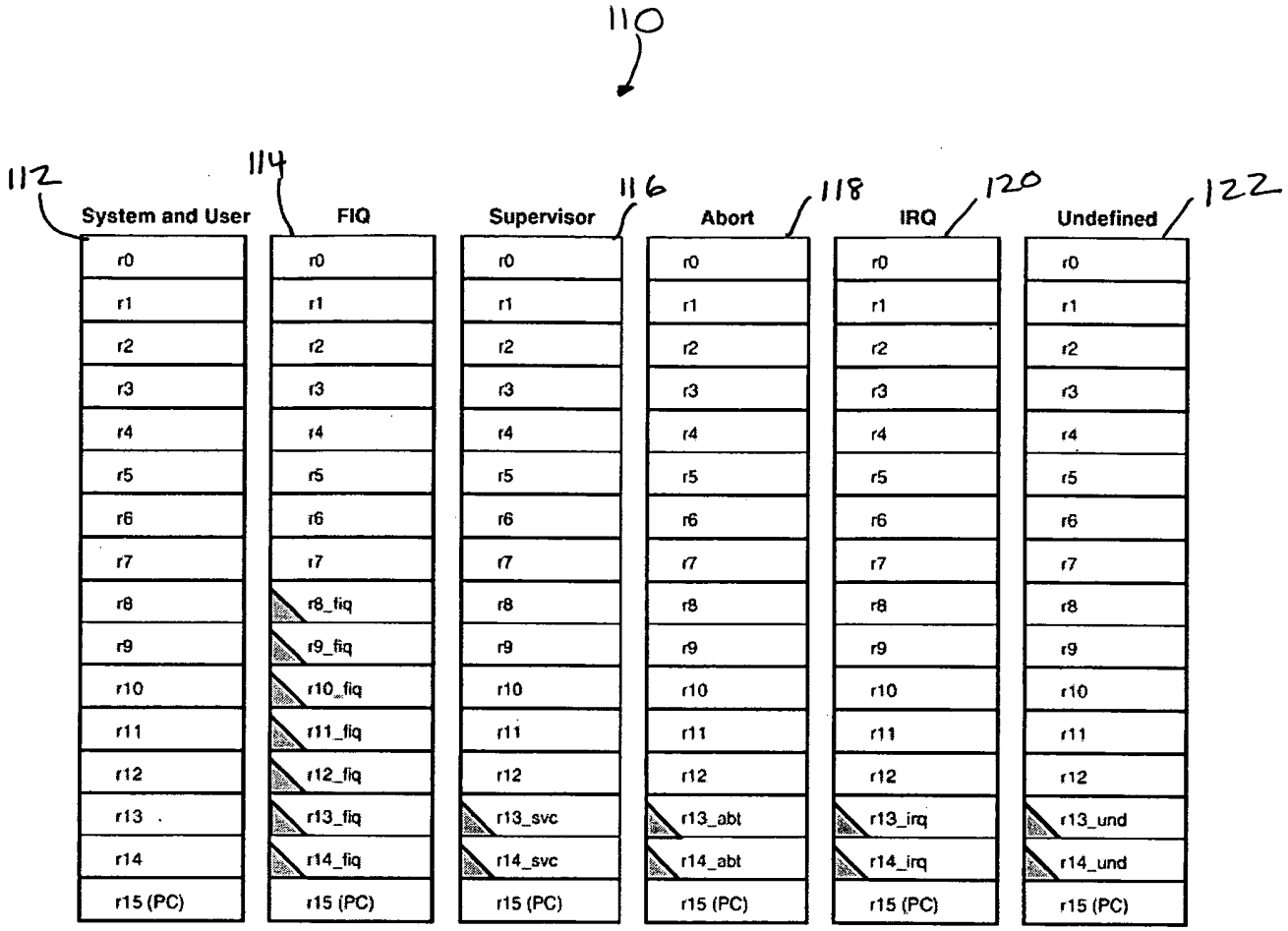
110
112
114
116
118
120
122
System and User
FIQ
Supervisor
Abort
IRQ
Undefined
r0
r1
r2
r3
r4
r5
r6
r7
r8
r9
r10
r11
r12
r13
r14
r15 (PC)
r8_fiq
r9_fiq
r10_fiq
r11_fiq
r12_fiq
r13_fiq
r14_fiq
r13_svc
r14_svc
r13_abt
r14_abt
r13_irq
r14_irq
r13_und
r14_und

Figure 2

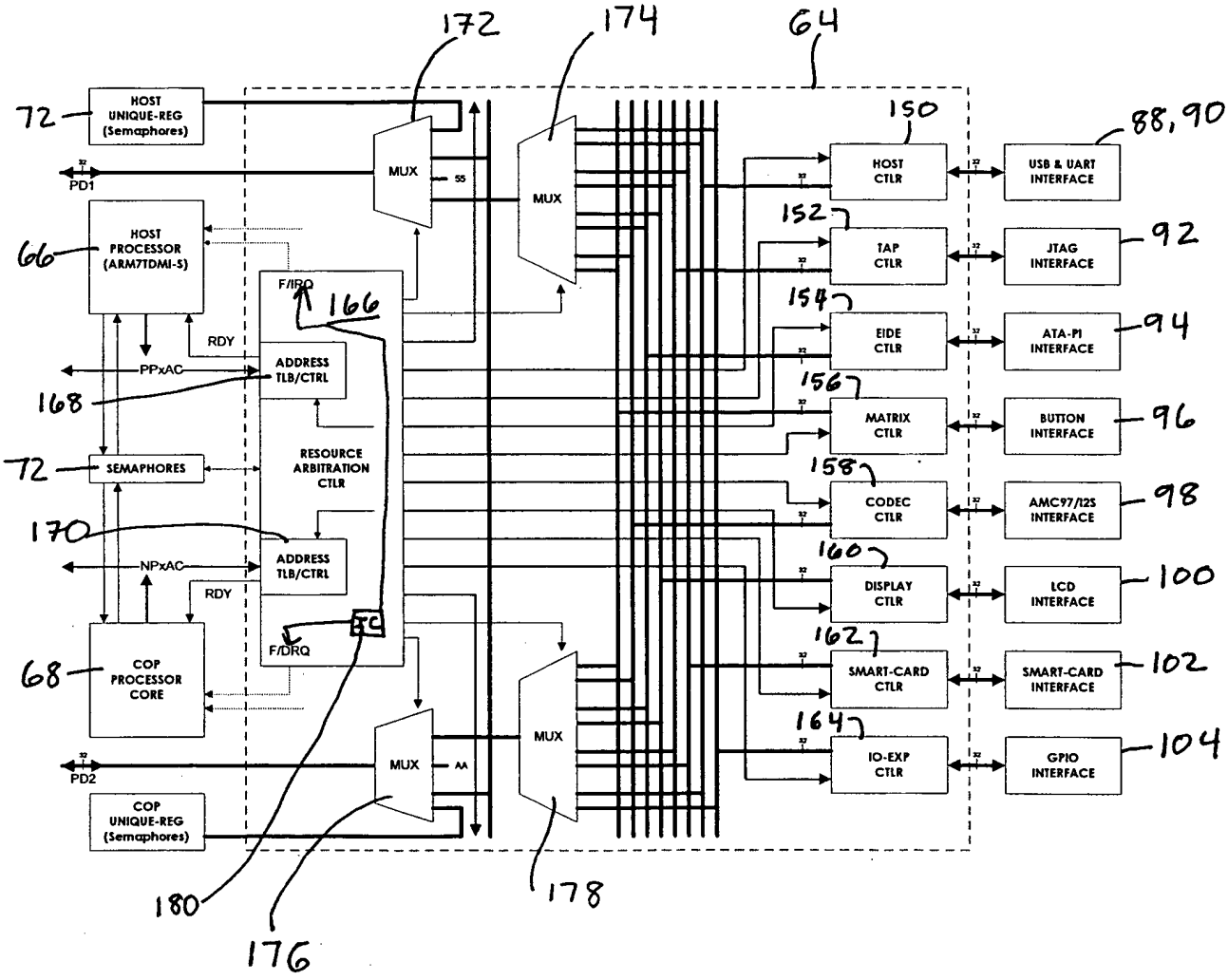
172
174
64
72
HOST UNIQUE-REG (Semaphores)
PD1
MUX
55
MUX
150
88,90
HOST CTLR
USB & UART INTERFACE
152
TAP CTLR
JTAG INTERFACE
92
66
HOST PROCESSOR (ARM7TDMI-S)
F/IRQ
166
154
EIDE CTLR
ATA-PI INTERFACE
94
RDY
PPxAC
ADDRESS TLB/CTRL
168
156
MATRIX CTLR
BUTTON INTERFACE
96
72
SEMAPHORES
RESOURCE ARBITRATION CTLR
158
CODEC CTLR
AMC97/I2S INTERFACE
98
170
NPxAC
ADDRESS TLB/CTRL
160
DISPLAY CTLR
LCD INTERFACE
100
RDY
F/DRQ
162
SMART-CARD CTLR
SMART-CARD INTERFACE
102
68
COP PROCESSOR CORE
164
IO-EXP CTLR
GPIO INTERFACE
104
MUX
AA
MUX
PD2
COP UNIQUE-REG (Semaphores)
180
178
176

Figure 3

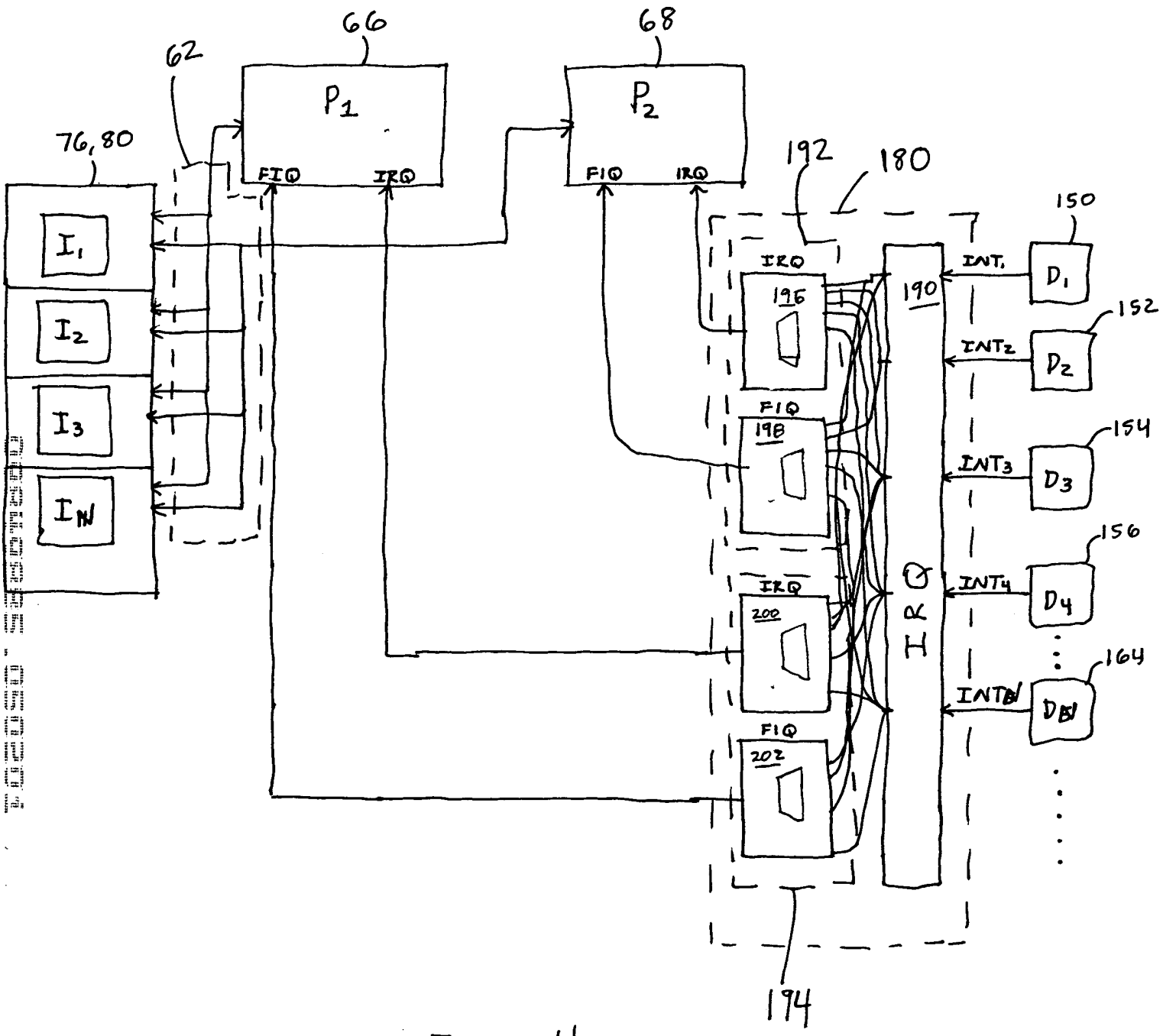
62
66
68
76, 80
P_1
P_2
FIQ
IRQ
192
180
150
I_1
I_2
I_3
I_N
IRQ
196
190
INT1
D_1
152
INT2
D_2
FIQ
198
154
INT3
D_3
156
IRQ
200
INT4
D_4
164
INTN
D_N
FIQ
202
194

Figure 4

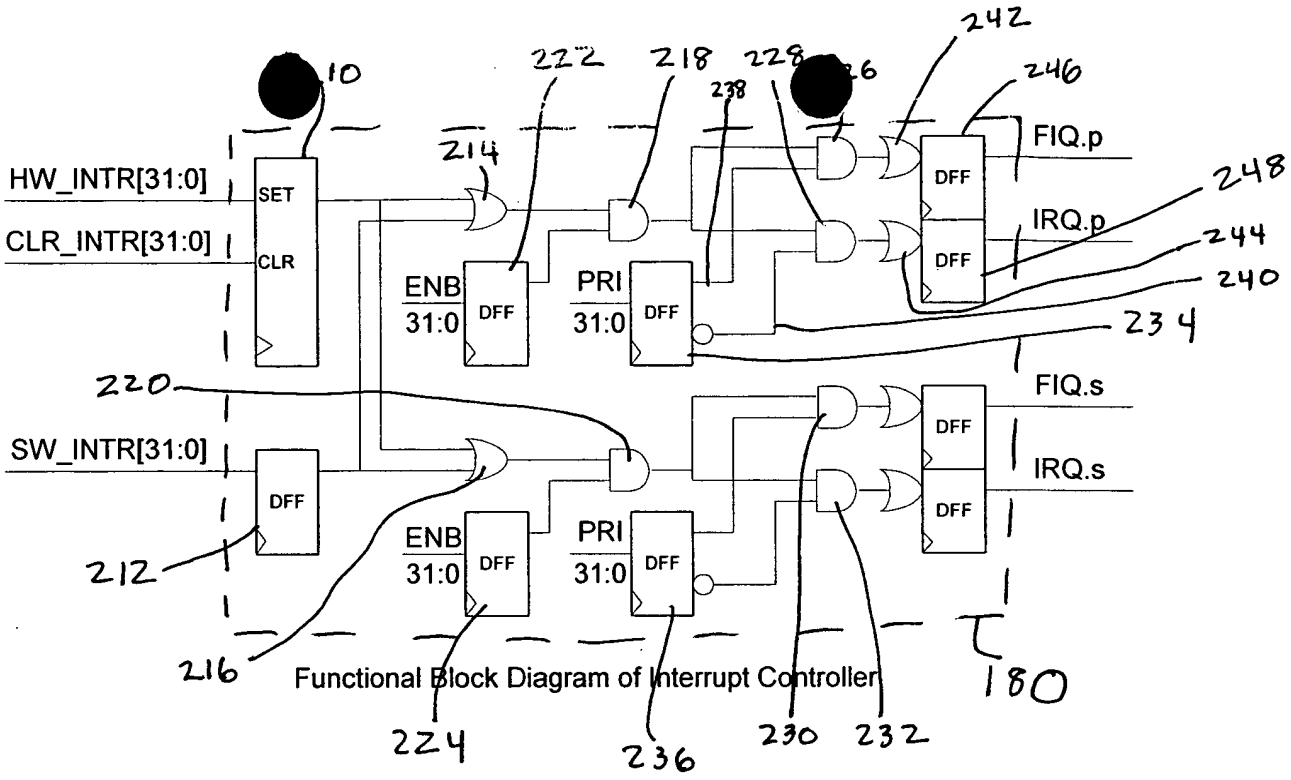

Figure 5

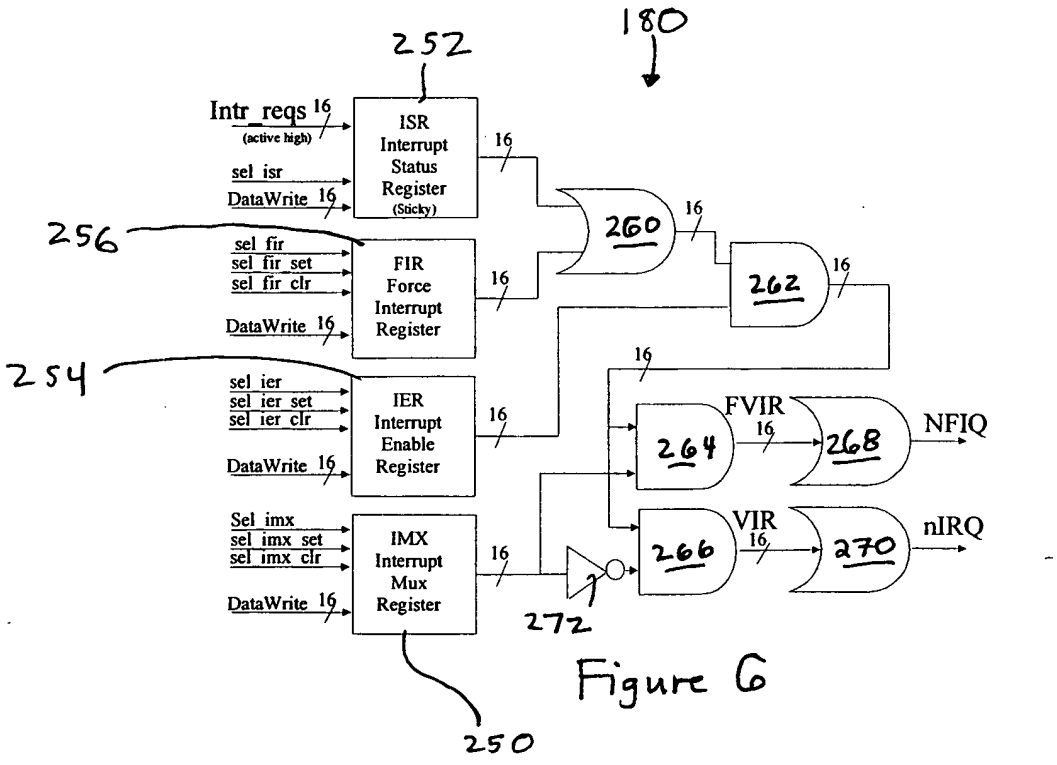

Figure 6

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Offset	Register	Description
0	ISR	Interrupt Status Register
4	IER	Interrupt Enable Register
8	IER_set	Each bit written as one will set the corresponding bit in IER
C	IER_clr	Each bit written as one will clr the corresponding bit in IER
10	FIR	Force Interrupt Register
14	FIR_set	Each bit written as one will set the corresponding bit in FIR
18	FIR_clr	Each bit written as one will clr the corresponding bit in FIR
1C	IMX	Interrupt Mux Register ('1/0' Routes interrupt to nFIQ/nIRQ)
20	IMX_set	Each bit written as one will set the corresponding bit in IMX
24	IMX_clr	Each bit written as one will clr the corresponding bit in IMX
28	VIR	Read only Valid Interrupt Register for nIRQ
2C	FVIR	Read only Fast Valid Interrupt Register for nFIQ

282

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Figure 7

Bit	Description
0	USB
1	UART A
2	UART B
3	External
4	USB Fast
5	Not Defined (CIF)
6	Not Defined
7	Not Defined (Keyboard)
8	EIDE 1
9	EIDE 2
A	Not Defined
B	Not Defined
C	Not Defined
D	Timer 2
E	Timer 1
F	Not Defined
10	USB Reset
11	AC
12	Timer 1
13	Timer 2
31:14	Not Defined

Figure 8

Interrupt Controller																							
VIRQ_CPU	CF00:1000	RO	32b	Valid Interrupt Status for CPU (primary)	00000000			IRQ31	IRQ30	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22
VIRQ_COP	CF00:1004	RO	32b	Valid Interrupt Status for COP (secondary)	00000000			IRQ31	IRQ30	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22
VFIQ_CPU	CF00:1008	RO	32b	FIQ Valid Interrupt Status for CPU (primary)	00000000			FIQ31	FIQ30	FIQ29	FIQ28	FIQ27	FIQ26	FIQ25	FIQ24	FIQ23	FIQ22
VFIQ_COP	CF00:100C	RO	32b	FIQ Valid Interrupt Status for COP (secondary)	00000000			FIQ31	FIQ30	FIQ29	FIQ28	FIQ27	FIQ26	FIQ25	FIQ24	FIQ23	FIQ22
ISR (read-only)	CF00:1010	RO	32b	Latched Interrupt Status Register (HW)	00000000			ISR31	ISR30	ISR29	ISR28	ISR27	ISR26	ISR25	ISR24	ISR23	ISR22
FIR (read-only)	CF00:1014	RO	32b	Forced Interrupt Status Register (SW)	00000000			FIR31	FIR30	FIR29	FIR28	FIR27	FIR26	FIR25	FIR24	FIR23	FIR22
FIR_SET	CF00:1018	set	32b	Force Interrupt Register Set	00000000												
FIR_CLR	CF00:101C	clr	32b	Force Interrupt Register Clear	00000000												
CPU_IER (read-only)	CF00:1020	RO	32b	Enabled Interrupt Source for CPU	00000000			IER31	IER30	IER29	IER28	IER27	IER26	IER25	IER24	IER23	IER22
CPU_IER_SET	CF00:1024	set	32b	Set Interrupt Source for CPU	00000000												
CPU_IER_CLR	CF00:1028	clr	32b	Clear Interrupt Source for CPU	00000000												
CPU_IEP_CLASS	CF00:102C	RW	32b	CPU's Interrupt Enable Priority Class (FIQ/IRQ)	00000000												
COP_IER (read-only)	CF00:1030	RO	32b	Enabled Interrupt Source for COP	00000000			IER31	IER30	IER29	IER28	IER27	IER26	IER25	IER24	IER23	IER22
COP_IER_SET	CF00:1034	set	32b	Set Interrupt Source for COP	00000000												
COP_IER_CLR	CF00:1038	clr	32b	Clear Interrupt Source for COP	00000000												
COP_IEP_CLASS	CF00:103C	RW	32b	COP's Interrupt Enable Priority Class (FIQ/IRQ)	00000000												
DMA_STATUS	CF00:1040	RO	32b	DMA Interrupt Source Status	00000000												

FIGURE 9A

IRQ21	IRQ20	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
IRQ21	IRQ20	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
FIQ21	FIQ20	FIQ19	FIQ18	FIQ17	FIQ16	FIQ15	FIQ14	FIQ13	FIQ12	FIQ11	FIQ10	FIQ9	FIQ8	FIQ7	FIQ6	FIQ5	FIQ4	FIQ3	FIQ2	FIQ1	FIQ0
FIQ21	FIQ20	FIQ19	FIQ18	FIQ17	FIQ16	FIQ15	FIQ14	FIQ13	FIQ12	FIQ11	FIQ10	FIQ9	FIQ8	FIQ7	FIQ6	FIQ5	FIQ4	FIQ3	FIQ2	FIQ1	FIQ0
ISR21	ISR20	ISR19	ISR18	ISR17	ISR16	ISR15	ISR14	ISR13	ISR12	ISR11	ISR10	ISR9	ISR8	ISR7	ISR6	ISR5	ISR4	ISR3	ISR2	ISR1	ISR0
FIR21	FIR20	FIR19	FIR18	FIR17	FIR16	FIR15	FIR14	FIR13	FIR12	FIR11	FIR10	FIR9	FIR8	FIR7	FIR6	FIR5	FIR4	FIR3	FIR2	FIR1	FIR0
FIR_SET (SET FORCED INTERRUPT BIT)																					
FIR_CLR (CLEAR FORCED INTERRUPT BIT)																					
IER21	IER20	IER19	IER18	IER17	IER16	IER15	IER14	IER13	IER12	IER11	IER10	IER9	IER8	IER7	IER6	IER5	IER4	IER3	IER2	IER1	IER0
CPU_IER_SET (ENABLE INTERRUPT SOURCE FOR CPU)																					
CPU_IER_CLR (DISABLE INTERRUPT SOURCE FOR CPU)																					
CPU_IEP_CLASS (SET PRIORITY INTERRUPT SOURCE FOR CPU)																					
IER21	IER20	IER19	IER18	IER17	IER16	IER15	IER14	IER13	IER12	IER11	IER10	IER9	IER8	IER7	IER6	IER5	IER4	IER3	IER2	IER1	IER0
COP_IER_SET (ENABLE INTERRUPT SOURCE FOR CPU)																					
COP_IER_CLR (DISABLE INTERRUPT SOURCE FOR CPU)																					
COP_IEP_CLASS (SET PRIORITY INTERRUPT SOURCE FOR CPU)																					
DMA_SOURCE_STATUS																					

Figure 9B

[9A][9B]